**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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**Ex parte** HIROSHI KAMIYAMA, MASATO SUZUKI and SHINYA MIYAJI

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Appeal No. 96-2446
Application 08/246,179[1]

_____

ON BRIEF

_____

Before KRASS, BARRETT and DIXON, **Administrative Patent Judges.**

DIXON, **Administrative Patent Judge.**

**DECISION ON APPEAL**

This is a decision on appeal from the examiner's final rejection of claims 1-12, which are all of the claims pending in this application.

[1]Application for patent filed May 19, 1994.

## BACKGROUND

The invention is directed to a data processing apparatus within a data processing system which allows data of various widths to be processed. The system includes an instruction decoder to decode the instruction, then the instruction is processed by the calculator/ALU. The system uses the conditional branch designation as a selector signal to select between the stored flag groups for the different size data. The system further uses the selected stored flag group to determine whether to perform a branch operation.

Appellants have indicated the grouping of the claims as Group I: claims 1-9; Group II: claims 10-11; and Group III: claim 12. Appellants have not clearly set forth separate arguments for patentability for each group as required by 37 CFR §§ 1.192(c)(7) and 1.192(c)(8)(iv). Appellants have only identified general benefits and have provided only explicit arguments to claim limitations which are expressly found in Claim 12 with respect to "simultaneously storing." All other arguments appear to be directed generally towards limitations found in independent claims 1, 10 and 12. Therefore, claims 1-11 will be considered as one group with representative claim 1. The second group will consist solely of claim 12.

Independent claim 1 is reproduced as follows:

1. An apparatus for processing data comprising:

an instruction decoding unit for decoding instructions, said instructions including arithmetic operation instructions and conditional branch instructions;

a calculator for operating N-bit data in accordance with decoded instructions, N being an integer;

a plurality of flag storage means, each of said plurality of flag storage means storing flag groups, each of said flag groups being changed based on a different bit width of N-bit data obtained by operation of said calculator;

a flag selecting means for selecting one of said plurality of flag storage means in accordance with an indication in a conditional branch instruction decoded by said instruction decoding unit; and

a branch judging unit for receiving a branch condition from a conditional branch instruction decoded by said instruction decoding unit and judging whether to branch, by referring to a flag group stored in a flag storage means selected by said flag selecting means.

Independent claim 12 is reproduced as follows:

12. An apparatus for processing data comprising:

an instruction decoding unit for decoding arithmetic operation instructions and conditional branch instructions;

a calculator for executing decoded instructions on data having a width of N-bits, N being an integer, to produce calculator results along with a plurality of flag groups, each flag group representing calculator results from a different bit width of data for later selecting an appropriate flag group;

storage means, for simultaneously storing the plurality of flag groups;

> flag selecting means for selecting an appropriate flag group in accordance with an indication of data bit width in a conditional branch instruction decoded by the instruction decoding unit; and
>
> a branch judging unit for obtaining a branch condition from a decoded conditional branch instruction and judging whether to branch, by comparing the branch condition to the appropriate flag group.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

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| Woods et al. (Woods) | 4,811,266 | Mar. 07, 1989 |
| Yamahata et al. (Yamahata) | 5,151,993 | Sep. 29, 1992 |

IBM Technical Disclosure Bulletin, Vol. 31, No. 2, issued July 1988, "Multiple Queued Condition Codes", pp. 294-96.

Claims 1-12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Woods in view of Yamahata and IBM.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and appellants, we make reference to the brief[2] and answer[3] for the details thereto.

## OPINION

After a careful review of the evidence before us we disagree with the Examiner that

[2] Appellants filed an appeal brief, November 20, 1995 (Paper No. 14). We will refer to this appeal brief as simply the brief.

[3] The Examiner responded to the brief with an Examiner's Answer mailed February 21, 1996 (Paper No. 15). We will refer to this examiner's answer as simply the answer.

claims 1-12 are properly rejected under 35 U.S.C. § 103 and we will not sustain the rejection of claims 1-12.

Turning to the rejection of claims 1-12, appellants argue "cited prior art teaches the coding of data width only in arithmetic instructions. Certainly the Examiner has been unable to cite any art disclosing data width being coded in conditional branch instructions or of data width decisions being deferred to the conditional branch decision." (See brief at page 9, paragraph 1.) We agree. Woods discloses that the flag data is available, but does not disclose that the flag data is stored in the manner as recited in claim language. The language of claim 1 requires "a **plurality** of flag storage means, **each** of said plurality of flag storage means storing flag storage **groups**, **each** of said flag groups being changed based on a different bit width of N-bit data obtained **by operation of said calculator**." (Emphasis added.) Woods does not disclose storing a plurality of flag groups and each flag group being changed based on a different bit width of N-bit data obtained by operation of said calculator. The claim language further requires "a flag selecting means for **selecting** one of said plurality of flag storage means **in accordance** with an indication **in a conditional branch instruction decoded by said instruction decoding unit**." (Emphasis added.) Woods discloses the selection of the appropriate flag data by use of control signals CTRL0 and CTRL1 to control the multiplexers. The flag group is formed therefrom. Moreover, the

control signals CTRL0 and CTRL1 which select the flag group do not select "in accordance with an indication in a conditional branch instruction" and are not "decoded by said instruction decoding unit" as required by the language of claim 1. Woods does not disclose that the instruction decoding unit produces control signals as required by the language of claim 1. The examiner states "Woods teaches the simultaneous production of a plurality of flag groups based on data width, and IBM teaches the saving of a plurality of flag groups. The selection of a flag group in IBM is deferred until a conditional branch instruction. These two references together sufficiently teach the Appellant[s'] invention." (See answer at page 7, paragraph 1.) We disagree. As discussed above, Woods does not disclose the storage of flag groups in plural storage means.

The Examiner argues "[r]egarding multiple data widths, the Examiner asserts that Woods and Yamahata, not IBM were relied upon to teach multiple data widths." (See answer at page 7, paragraph 3.) We note that the discussion in the answer with respect to Yamahata is limited to "Yamahata discloses a system with varying bit widths that explicitly teaches an instruction decoder." The Examiner has not provided a convincing line of reasoning why it would have been obvious to one of ordinary skill in

the art at the time of the invention to incorporate the teachings of Yamahata with those of Woods and IBM. It is unclear how Yamahata is to be combined with the teachings of

Woods and IBM. Moreover, the last sentence of paragraph one on page 8 of the answer states "[t]he combination of these two references [Woods and IBM] would yield a system that simultaneously stores a plurality of flag groups and then selects one of those flag groups based upon a conditional branch instruction." The rejection is based upon a combination of all three of the references and the Examiner has not provided the motivation to combine all of the teachings. The Examiner also states at page 7, line 5 of the answer that "[t]hese two references [Woods and IBM] together sufficiently teach the Appellant[s'] invention." From a review of the record as a whole, it is unclear whether all three of the references are being combined in the rejection and how the combination meets all the limitations of the claimed invention.

Appellants argue that IBM does not supply the teachings which are lacking in Woods. (See brief at page 9.) Appellants argue that the conditional branch instructions of IBM are not used to specify data width and IBM does not suggest the use of conditional branch instructions to specify data width. We agree. Appellants argue that IBM does not "simultaneously save a plurality of flag groups." We agree, but find this limitation only in claim 12. This limitation is not explicitly recited in claims 1 and 10, and

we will not read the limitation into these claims. It is axiomatic that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation

consistent with the specification, and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. ***In re Sneed***, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). Moreover, limitations are not to be read into the claims from the specification. ***In re Van Geuns***, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) citing ***In re Zletz***, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Appellants have set forth claims 1-9 in "means plus function" format, but have provided no argument as to any structure, materials or acts described in the specification or their equivalents required for a proper interpretation of the claimed "means." Therefore, we do not find that the language of claims 1 and 10 require "simultaneous storing" as explicitly recited in the language of claim 12.

We find that the examiner has not met the burden of setting forth a ***prima facie*** case of obviousness in rejecting claims 1-12. Our reviewing court has stated that obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." ***In re Keller***, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ***ACS Hosp. Sys., Inc. v. Montefiore Hosp.***, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). And "teachings of

references can be combined only if there is some suggestion or incentive to do so." ***Id***. Here, the prior art contains neither a teaching nor a suggestion to store plural flag groups which are changed based upon operation of the calculator. Furthermore, the examiner has provided no motivation as to why it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of IBM regarding processing conditional branch instructions and to modify the teachings of Woods to use the conditional branch instruction to select the appropriate stored flag group as set forth in claim 1. The examiner has attempted to find the parts of the claimed invention in rejecting the claims and has not considered the claim as a whole in evaluating patentability.

Instead, it appears to us that the examiner relied on hindsight in reaching the obviousness determination. However, our reviewing court has said, "[t]o imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." ***W. L. Gore & Assoc. v. Garlock, Inc.***, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983).

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the

respective positions articulated by the appellants and the Examiner. Upon evaluation of all the evidence before us, it is our conclusion that the evidence adduced by the examiner is not sufficient to establish a ***prima facie*** case of obviousness with respect to claim 1. Accordingly, we will not sustain the Examiner's rejection of claim 1 under 35 U.S.C. § 103.

Claim 10 contains similar limitations to claim 1 with respect to "a plurality of flag storage units each storing flag groups to be changed based on different bit widths in an operation result" and "changing said flag groups based on a data width of a calculating operation result produced by said calculator" and "selecting a selected flag group corresponding to a data width designated by a decoded branch instruction."

Claim 12 contains limitations similar to claim 1 with respect to "a calculator . . . to produce calculator results along with a plurality of flag groups" and "flag selecting means for selecting an appropriate flag group in accordance an indication of data bit width in an conditional branch instruction decoded by the instruction decoding unit."
Claim 12 further recites the limitation "simultaneously storing the plurality of flag groups."

Since all the limitations of independent claims 1, 10 and 12 are not taught or suggested by the applied prior art, we cannot sustain the Examiner's rejection of appealed claims 2-9 and 11 which depend therefrom, under 35 U.S.C. § 103.

**CONCLUSION**

To summarize, the decision of the Examiner rejecting claims 1-12 under 35 U.S.C.

§ 103 is reversed. The decision of the Examiner is reversed.

**REVERSED**

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| ERROL A. KRASS | ) | |
| Administrative Patent Judge | ) | |
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| | ) | BOARD OF PATENT |
| LEE E. BARRETT | ) | APPEALS AND |
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